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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/696,920	10/30/2003	Jung Pill Kim	2003P52789US	8247

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GERO G. MCCLELLAN
MOSER, PATTERSON & SHERIDAN, L.L.P.
Suite 1500
3040 Post Oak Blvd.
Houston, TX 77056

EXAMINER	
NGUYEN, LINH M	
ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 08/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/696,920	KIM ET AL.	
	Examiner	Art Unit	
	Linh M. Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,5-14,16-18 and 20-27* is/are rejected.

7)☒ Claim(s) *3,4,15 and 19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is a reply to the Applicant's response submitted on 07/19/2004. By virtue of this response, claims 1-27 are now pending.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

2. Claims 1-2, 5-13 and 22-27 are rejected under 35 U.S.C. 102(e) as being anticipated by Saeki (U.S. Pub. No. 2002/0079938).

With respect to claims 1 and 22, Saeki discloses, in Figure 6, a phase blending circuit and a corresponding method for generating a plurality of signals differing in phase relative to an early phase signal comprising a) a current source [MP51] having a common output node [common node at drain of MP51]; b) one or more delay elements [C1,..., C8; MN11,..., MN2N], and c) one or more switches [MN51, ..., MN58, MN31,..., MN4N] to selectively couple one or more of the delay elements to the common output node of the current source,

wherein a time required for a voltage level at the common output node to fall below a threshold level after assertion of the early phase signal is dependent on which of the one or more delay elements are coupled to the common output node.

With respect to claims 2 and 24, Saeki discloses, in Figure 6, that the one or more delay elements comprises at least one transistor [MN11,..., MN2N] to provide a path for current flow from the common output node of the current source in response to assertion of the early phase signal.

With respect to claim 5, Saeki discloses, in Figure 6, that the one or more delay elements comprises at least one capacitor [C1,..., C8] coupled to the common output node of the current source.

With respect to claim 6, Saeki discloses, in Figure 6 and paragraph [0067], last three lines, that the at least one capacitor comprises a plurality of capacitors having different values of capacitance.

With respect to claim 7, Saeki discloses, in Figure 6, that the capacitor values are selected such that the phases of the plurality of signals are separated by a substantially equal phase.

With respect to claim 8, Saeki discloses, in Figure 6, a phase blending circuit comprising a) a current source [MP51] having a common output node and a control input [output from OR51] for disabling the current source when a late phase signal trailing the early phase signal is asserted; b) a comparator [INV51] having an input coupled with the common output node of thecurrent source; c) a plurality of delay elements [C1,..., C8; MN11,..., MN2N], d) a path for current flow from the common output node when the early phase signal is asserted; and a plurality of switches [MN51, ..., MN58, MN31,..., MN4N] to selectively couple one or more of

the delay elements to the output node of the current source for varying the time required for a voltage level of the common output node to fall below a threshold level as a result of current flow through the path.

With respect to claim 9, Saeki discloses, in Figure 6, that the path for current flow comprises at least one transistor [MN11, ..., MN2N] receiving the early phase signal as an input.

With respect to claim 10, Saeki discloses, in Figure 6, that the at least one transistor is one of the delay elements [MN11, ..., MN2N] coupled to the common output node of the current source via one of the switches [MN31,..., MN4N].

With respect to claim 11, Saeki discloses, in Figure 6, that the at least one transistor comprises an NMOS transistor [MN11, ..., MN2N] and the current source comprises a PMOS transistor [MP51].

With respect to claim 12, Saeki discloses, in Figure 6, that 12 the path for current flow further comprises at least one transistor [MN11, ..., MN2N] receiving the late phase signal as an input.

With respect to claim 13, Saeki discloses, in Figure 6, that the one or more delay elements are configured to allow generation of a plurality of signals having phases separated by a substantially equal phase.

With respect to claim 23, Saeki discloses, in Figure 6, the step of coupling the late signal to a control input [output from OR51] of the current source to disable the current source [MP51] for disabling the current source when a late phase signal is asserted.

With respect to claim 25, Saeki discloses, in Figure 6, that the one or more switches [MN51, ..., MN58, MN31, MN4N] comprise one or more transistors.

With respect to claim 26, Saeki discloses, in Figure 6, that the one or more delay elements comprise one or more capacitors [C1, ..., C8] comprise one or more transistors.

With respect to claim 27, Saeki discloses, in Figure 6, that the late signal trails the early signal by a unit delay; and the switches [MN51, ..., MN58, MN31,..., MN4N] and delay elements [C1,..., C80; MN11,..., MN2N] are configured to provide the delayed signal differing in phase from the early signal by a fraction of the unit delay, wherein the fraction depends on which of the switches are closed.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 14 and 16-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (Fig. 1) in view of Saeki (U.S. Pub. No. 2002/0079938).

With respect to claims 14 and 16-17, Applicant Admitted Prior Art discloses, in Fig. 1, a delay locked loop circuit for generating an output signal aligned with an input signal comprising a) a delay line [102] for providing phase signals delayed relative to the input signal [CK in] by one or more of unit delays, b) a phase blending circuit [108] for generating a blended phase signal and c) control logic configured to monitor skew between the input and output signals and, based on the skew, generate one or more control signals to select the early and late signals provided to the phase blending circuit and to selectively couple one or more of the delay elements to a common output node.

Applicant Admitted Prior Art fails to disclose a specific configuration of the claimed phase blending circuit including a current source having a common output node, one or more delay elements, one or more switches to selectively couple one or more of the delay elements to the common output node of the current source, wherein a time required for a voltage level at the common output node to fall below a threshold level after assertion of the early phase signal is dependent on which of the one or more delay elements are coupled to the common output node, a comparator having an input node coupled with the common output node of the current source, and the threshold level is the threshold level of the comparator and the output signal is generated on an output node of the comparator.

Saeki discloses, in Fig. 6, a phase blending circuit for generating a plurality of signals differing in phase relative to an early phase signal comprising a) a current source [MP51] having a common output node [drain of MP51]; b) one or more delay elements [C1,..., C8; MN11,..., MN2N], c) one or more switches [MN51, ..., MN58, MN31,..., MN4N] to selectively couple one or more of the delay elements to the common output node of the current source, wherein a time required for a voltage level at the common output node to fall below a threshold level after assertion of the early phase signal is dependent on which of the one or more delay elements are coupled to the common output node, d) a comparator [INV51] having an input node coupled with the common output node of the current source, and the threshold level is the threshold level of the comparator and e) the output signal is generated on an output node of the comparator.

To configure the circuit of Applicant Admitted Prior Art, Fig. 1, with a phase blending circuit with a specific detailed description as addressed above and taught by Saeki to provide synchronization between the input signal and the reference clock would have been obvious to

one of ordinary skill in the art at the time of the invention since such configuration with the phase blending circuit is used for maintaining clocks input to a plurality of circuits in an integrated circuit in synchronization.

5. Claims 18 and 20-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kwak (U.S. Patent No. 6,646,939) in view of Applicant Admitted Prior Art (Fig. 1) and Saeki (U.S. Pub. No. 2002/0079938).

With respect to claim 18, Kwak discloses, in Fig. 1, a dynamic random access memory (DRAM) device comprising a) one or more memory elements [60,70]; and b) a delay locked loop circuit [20] for synchronizing data output from the one or more memory elements with a clock signal.

Kwak fails to disclose a detailed description of the delay locked loop including (a) a delay line, (b) a phase blending circuit comprising a current source and one or more delay elements for selectively coupling to a common output node of the current source, in which a time required for a voltage level at the common output node to fall below a threshold level after assertion of an early phase signal provided by the delay line is dependent on which of the one or more delay elements are coupled to the common output node, and (c) control logic configured to monitor skew between the input and output signals and, based on the skew, generate one or more control signals to select the early signal provided to the phase blending circuit by the delay line and to selectively couple one or more of the delay elements to the common output node.

Applicant Admitted Prior Art, Fig. 1, discloses a delay locked loop including (a) a delay line, (b) a phase blending circuit, and (c) control logic configured to monitor skew between the input and output signals and, based on the skew, generate one or more control signals to select

the early signal provided to the phase blending circuit by the delay line and to selectively couple one or more of the delay elements to the common output node.

Applicant Admitted Prior Art, Fig. 1, lacks to disclose details of the phase blending circuit.

Saeki discloses a phase blending circuit comprising a current source and one or more delay elements for selectively coupling to a common output node of the current source, in which a time required for a voltage level at the common output node to fall below a threshold level after assertion of an early phase signal provided by the delay line is dependent on which of the one or more delay elements are coupled to the common output node; in which one or more delay elements comprises a plurality of capacitors [C1, ..., C8] and they are of the same type as capacitors utilized in the memory elements.

It would have been obvious to one of ordinary skill in the art at the time of the invention to configure the circuit of Kwak with a delay locked loop as taught in Applicant Admitted Prior Art, Fig. 1, including a) a delay line, b) a phase blending circuit and c) a control logic to provide sufficient synchronization between the input clock signal and the output clock signal since such circuit arrangement of the logic circuit for the stated purpose has been a well known practice as evidenced by the teachings of Applicant Admitted Prior Art, Fig. 1 *(see Specification, [0003]).*

Furthermore, to configure the circuit of the combination of Kwak and Applicant Admitted Prior Art (Fig. 1) with a phase blending circuit, as taught by Saeki with all the details indicated in the previous paragraph, to maintain synchronization between the input signal and the reference clock would have been obvious to one of ordinary skill in the art at the time of the

invention since Saeki teaches that the phase blending circuit is used for maintaining clocks input to a plurality of circuits in an integrated circuit in synchronization.

Allowable Subject Matter

6. Claims 3-4, 15 and 19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

11. The following is a statement of reasons for the indication of allowable subject matter:

The closest prior art on record does not show or fairly suggest:

a) The phase blending circuit, in which the at least one transistor comprises a plurality of transistors having different dimensions, as called for in claim 3;

c) The delay locked loop circuit, in which the control logic is further configured to:

- determine if the input and output signals are aligned within an accepted tolerance,
- if not, modify the one or more control signals to couple a different one or more of the delay elements to the common output node; and
- repeat steps (a)-(b) until the input and output signals are aligned within the accepted tolerance,

as called for in claim 15;

d) The DRAM device, in which the one or more delay elements comprise a plurality of transistors having different dimensions, as called for in claim 19.

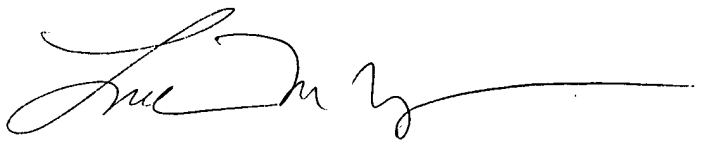
Inquiry

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh M. Nguyen whose telephone number is (571) 272-1749. The examiner can normally be reached on Alternate Mon, Tuesday - Friday from 7:00 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LMN



LINH MY NGUYEN
PRIMARY EXAMINER